Integrated Adaptive LO Leakage Cancellation for W-CDMA Direct Upconversion Transmitters

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Abstract — **A method for on-chip implementation is presented to compensate both local oscillator leakage due to finite LO to RF port isolation and input DC offset. It uses an RF power detector and a digital control loop and is intended for use in direct upconversion transmitters. The entire control loop was integrated in a CMOS UMTS transceiver chip. This paper presents the cancellation principle, simulations, and measurement results.**

I. Introduction

A common problem in modern communication systems is that the local oscillator (LO) signal required for the modulator leaks to the output [1]. Reasons for this phenomenon are the nonideal isolation between LO and RF port (crosstalk), a unavoidable DC offset voltage at the modulator's input ports due to mismatches and imperfections in the baseband components [2], and mixer unbalances caused by process variance.

There are two main reasons to limit this leakage. First, technical specifications for mobile communication system (e.g. UMTS) define a frequency mask. The leakage must not cause illegal inband spurious emissions. Second, an unwanted carrier component at the RF port can worsen the linearity of the amplifier because of higher signal levels. In heterodyne transmitters the LO feedthrough can mostly be eliminated by the use of proper frequency planning and filtering, whereas in broadband systems the RF and LO bands often happen to overlap each other. This is obviously always the case for homodyne transmitters. There are several methods to handle LO leakage. Balancing techniques [1] are frequently used. However, tolerances rarely allow more than 30 dB suppression of the LO leakage (LOL). Another possibility is to add a correctly leveled and phase shifted part of the LO signal to the RF signal [3]. This procedure requires very complex mixers. The goal of this work was to develop a simple, robust, and easy to implement algorithm for canceling LO leakage. In Chapter II the novel method and its building blocks are described. Chapter III deals with the specifications of the components. In Chapter IV simulation results are presented, and finally in Chapter V the verification results are shown.

II. Description of the Method

A. Principle

A DC voltage at the mixer input causes an RF signal corresponding to the local oscillator signal. The sign of the input voltage decides either the RF signal is opposite-phase or in-phase to the LO signal. The amplitude of the RF signal depends on the amplitude of the offset voltage. The output generated in this manner adds to the unwanted LO leakage, thus providing the possibility for cancellation [4].

A simple method to find the proper input voltage for minimized LO leakage power is successive approximation: starting at the maximal input voltage provided by the controller, the offset is decreased step by step by means of adjusting the DC voltage at the mixer input until the leakage is minimal. This requires an RF power detector to be included with an output DC voltage corresponding to the input RF power as can be seen in Fig. 1. A digital controller decreases the offset voltage as long as the power detector output voltage does not rise. As there is only one power minimum within the adjustable range at the optimal offset voltage, convergence is guaranteed.

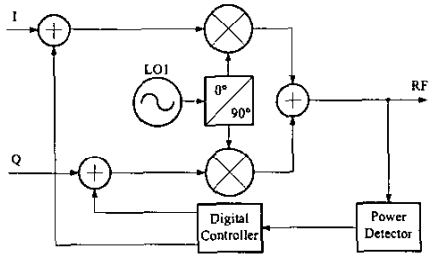

Fig. 1. Principle of the feedback loop.

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Because an I/Q-Modulator has two baseband input ports the optimization process has to be performed twice. First, the proper offset voltage for the in-phase input is determined, and second, the quadrature input offset is adjusted to get the ultimate LO leakage suppression. As the power changing near the optimum in-phase offset voltage is quite low in the case of a relatively high quadrature offset, the loop sensitivity for the first in-phase compensation can be bad, another in-phase optimization after the quadrature compensation may be necessary.

The LO leakage minimization process can be started once if the chip is switched on and repeated if necessary when there is no transmission.

B. RF Power Detector

To find the point with the optimal input offset voltage one has to keep tab on the modulator's output power. The power is reduced with each step coming closer to the optimal input offset. Exceeding the optimum, the RF power would start to increase again. Therefore, demands on the detector are an RF input port covering the full expected output power of the modulator and a strictly monotonic decreasing characteristic to avoid local minimums. An example for a valid power detector behavior is plotted in Fig. 3. There are several known detector circuits [5]: via thermo elements, thermistors, FET's or Schottky diodes.

C. Digital Controller

The digital controller mainly consists of a register, a comparator, and a counter. Additionally, an A/D-converter and a D/A-converter are necessary. The step size of the output D/A-converter depends on the wanted extra LO suppression. The smaller the step size, the closer the optimal offset voltage can be reached. The number of steps, respectively the resolution, depends on the expected offset without optimization and the chosen step size. To specify the input A/D-converter the RF detector's characteristic has to be taken into account. As this curve flattens in the lower range, the LSB voltage has to be small enough to detect the tiny changes close to the minimum of the modulator's output power to prevent untimely aborts of the approximation. The required number of bits can be calculated regarding the detector output voltage at the maximum output power of the modulator [6].

Time delay gates with a considerably small delay time compared to the clock period have to be inserted (see Fig. 2) to ensure proper clocking of several elements of the digital controller in the correct order. At first the A/D-converter is triggered to convert the voltage. Then the comparator compares the new value to the old one saved in the register and decides whether the voltage has been

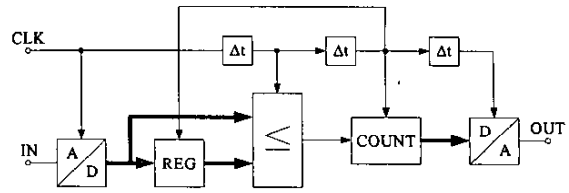

Fig. 2. Digital controller.

reduced. If so, the counter is decreased. The digitized value can be shifted into the register at the same time. The counter output is D/A-converted and represents the new offset voltage. These steps are repeated until the RF power starts to rise again. The maximum clock frequency primary depends on the cut-off-frequency of the power detector.

III. Design Values

A. I/Q-Modulator

For simulations and measurements the conversion gain of the UMTS compliant direct upconversion modulator was set to 0 dB. The local oscillator's power was 0 dBm at a frequency of 2 GHz.

B. Power Detector

The expected LO leakage power is −30 dBm, corresponding to an LO power of 0 dBm and a suppression without feedback loop of approximately 30 dB. Goal of the feedback loop is to suppress the LO leakage power down to at least −55 dBm. Therefore the power detector has to convert an RF input power from at least −55 dBm to −30 dBm into a equivalent DC voltage. For simulations a power detector with an input range of −70 dBm to −20 dBm and a DC output voltage of 0.25 V up to 1.3 V was used (see Fig. 3).

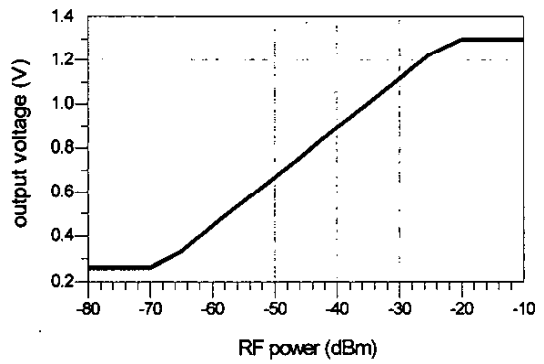

Fig. 3. Power detector characteristics.

C. D/A-Converter

Assuming that the total LO leakage without any compensation is −30 dBm, the corresponding input offset voltage V_{DCMAX} calculates to 20 mV (R = 200 Ω).

$$V_{DCMAX} = \sqrt{2 \cdot 200\Omega \cdot 10^{\frac{-30\,dBm-30}{10}}} = 20\,mV \qquad (1)$$

If we want to suppress the LO leakage to −55 dBm we can determine the maximum step size of the offset voltage [7]:

$$V_{DCSTEPMAX} = \frac{1}{2}\sqrt{200\Omega \cdot 10^{\frac{-55\,dBm-30}{10}}} = 0.4\,mV \qquad (2)$$

With these results we can specify the D/A-converters at the output of the digital controller: For the simulations and implementation described below a 7 bit D/A-converter with a step size of 0.35 mV was chosen. Thus, the I and Q input offset voltages are adjustable from -22.4 mV to 22.4 mV.

D. A/D-Converter

For simulations and implementation a 10 bit A/D-converter (successive approximation principle) with an input range of 0.25 V to 1.3 V was used.

IV. Simulation Results

Simulations were performed using the parameters calculated above. The optimization process is started at t_0 as can be seen in Fig. 4. The output power raises abruptly because of the additional DC offset at the modulator's input ports due to the digital controller.

Step by step the power decreases as the I offset voltage gets closer to its optimal value. As soon as there is no more detectable power change (t_1) then Q offset voltage starts to decrease until the power minimum is reached (t_2).

V. Measurement Results

The entire feedback loop was integrated in a recently developed 0,12 µm CMOS single chip UMTS transceiver [7]. An on-chip multistage FET rectifier is used for power detection, the output voltage is digitized by a 10-bit ADC. Two 7-bit DACs are integrated in the baseband filters. Without any compensation the test chip has an LO leakage power of −30 dBm. Using the digital feedback loop presented in this work it is possible to suppress the LO leakage power by another 28 dB down to −58 dBm.

The different offset voltage step size recognizable in Fig. 5 is caused by process inaccuracy (transistor imbalances).

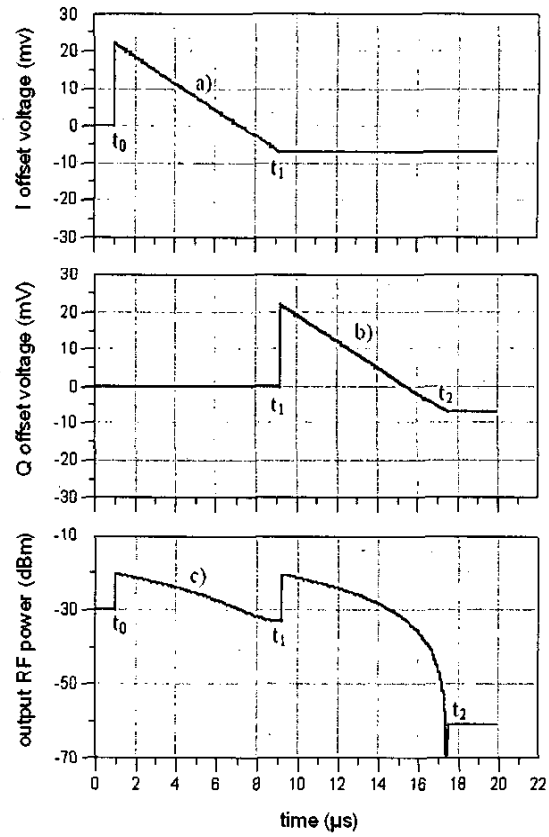

Fig. 4. Simulation results:
a) Input voltage at in-phase input port.
b) Input voltage at quadrature input port.
c) Output RF power.

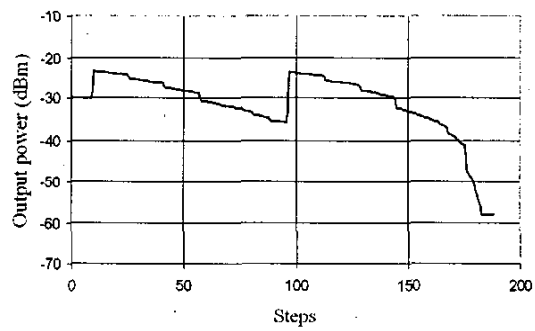

Fig. 5. Measurement results.

VI. SUMMARY

A fully integrated feedback loop for local oscillator leakage cancellation was presented in this work. Simulation results show that the principle works robustly. Measurements were done to verify the simulation results.

The development of the test chip is still in progress, further improvements of LO leakage suppression are expected.

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